FPGA-based time counters with a wander measurement mode

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Abstract* – *This paper presents the design and basic technical features of the series of virtual time interval counters with a wander measurement mode. The counters are developed as computer card with PCI interface and as portable modules with USB or Wi-Fi interfaces. The measurement functions are executed by the time counter unit integrated in an FPGA device. To achieve high precision and wide measurement mode a two-stage interpolation method is used. The precise and fast time-to-digital (T/D) conversion in the second stage of interpolation is performed with the aid of carry chains built-in the FPGA chip. The use of up to 16 such chains in a single interpolator leads to the high measurement resolution of 1.2 ps. The short death time of T/D converters allowed to introduce several specialized measurement modes, and among them the wander measurement.

Keywords—time interval counter, two-stage interpolation, wander measurement

I. INTRODUCTION

The modern microelectronic technology allows to develop of high-precision, low-cost time interval counter as a single FPGA (*Field Programmable Gate Array*) device [1–5]. Typically in such a time counter a tapped delay line is used for T/D conversion. Thus the resolution of conversion is limited by the propagation time of a single delay element. To increase the resolution two shifted delay lines [6] or independent delay lines [7] may be used. The highest resolution and precision are provided in time counters combining the two-stage interpolation and multiple independent delay lines [8]. To make such integrated counters easy applicable and more useful for average user we considered their possible applications and designed three models of virtual time counters in the forms of a computer card and small portable modules. They differ each other mainly with respect to the computer interface. The computer card is equipped with the PCI interface, while portable modules have USB or Wi-Fi interface.

Precise time interval measurements are crucial in many areas of research and industry. In telecommunication, slow variations in signal timing through a system (*wander*) are investigated [9–12]. Due to these needs we introduced the specialized operation modes of the counter, including measurement of Time-Interval Error (TIE) and Time Deviation (TDEV). Each developed counter is controlled by a user-friendly software working in the Windows environment and creating a virtual front-panel of the counter on the monitor screen.

In this paper we describe the design of the integrated counter chip, its operation in the wander measurement mode and the respective technical details. We also present the results of some performed tests.

II. INTERPOLATION METHOD

The wide measurement range and high resolution in the advanced integrated time counters are obtained by the use of two-stage interpolation method (fig. 1). The wide range of the measured time intervals T is achieved by counting an integer number N of the reference clock periods T_0, whose leading pulse edges appear at the counter inputs between the leading edges of the START and STOP pulses. These pulses represent, respectively, the begin and end of the measured time interval T. Then the product NT_0 is calculated giving a rough estimate of the T. The higher resolution is provided by two two-stage interpolators, one on each input channel, which precisely measure the fractional parts of T within single clock periods. In the First Interpolation Stage (FIS) of each interpolator a multiphase clock is commonly used. In our case we applied Four Phase Clock (FPC). The FIS detects in which segment of FPC the input pulse START (STOP) appears that allows to evaluate of T_{ST1} (T_{SP1}). Simultaneously, the time interval T_{ST2} (T_{SP2}) between the START (STOP) pulse and the nearest edge of the FPC is measured in the Second Interpolation Stage (SIS). The final measurement result is calculated as:

$$T = NT_0 + (T_{ST1} + T_{ST2}) - (T_{SP1} + T_{SP2}) \qquad (1)$$

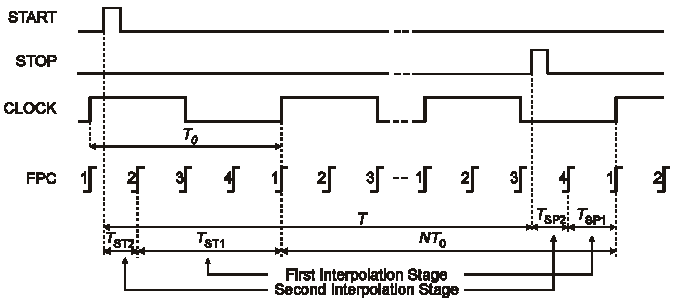

Figure 1. Two-stage interpolation method

This work was supported by the Polish National Science Centre under contract no. DEC-2011/01/B/ST7/03278

III. TIME COUNTER

The block diagram of time counter based on the two-stage interpolation method is shown in figure 2. The FIS detects the FPC segment in which an input pulse (START or STOP) appears and synchronizes the latter with the nearest FPC edge. This edge is then used both to enable the main counter and for precise conversion in the SIS. A synchronizer is needed to ensure proper work of the main counter. The results from FIS and SIS are converted to NB code and then they are transferred to the code processor. This processor executes the statistical code density test [13], performed for identification of the nonlinearity of interpolator, calculates and stores the resulting transfer characteristic. The measurement results from interpolator are calculated and corrected on-the-fly in that block as well.

To obtain high measurement rate and minimize the dead time between successive measurements a FIFO memory in the FPGA device is used. It allows increasing the maximum measurement rate up to 5 million measurements per second (when measuring the "zero time interval").

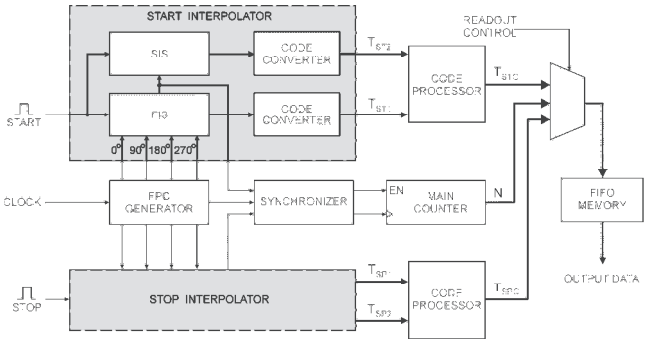

Figure 2. Block diagram of the time counter

A simple FPC generator can be built as a tapped delay line. Such line consists of few logic gates, which have appropriate delays to obtain required clock phase segments. As the paths delays are crucial to achieve high uniformity of the clock segments, the manual routing is needed.

For precise T/D conversion within a single phase segment of the FPC, tapped delay line is used. It consists of multiplexers forming the fast carry chains in FPGA devices. Such multiplexers offer the shortest propagation time among all logical elements available in programmable devices. Due to recent improvement in CMOS technology the delay of a single multiplexer improved from tens of picoseconds (45 ps – *Spartan-3*) to several picoseconds (19 ps – *Spartan-6*). To further improve the delay line resolution beyond its cell delay we proposed to use multiple independent delay lines for creating an equivalent coding line [7, 8]. In this way the *n*-delay lines increase the resolution of about *n*-times.

Figure 3 shows the external view of the computer card (left) and the portable module (right). The FPGA counter is located in the center of the card (yellow label) and below is the PCI interface chip.

Figure 3. External view of the counter board with PCI interface and the counter module with USB nterface

IV. MEASUREMENT MODES

The counter can operate either in the calibration mode or in the measurement modes. The calibration is performed automatically in two consecutive procedures. In the first one, the transfer characteristics of interpolators are identified. In the second one, the time offset between two input channels (START and STOP) is calculated.

Each of five measurement modes may be selected by clicking the predefined virtual keys on the virtual front panel of the counter (fig. 4).

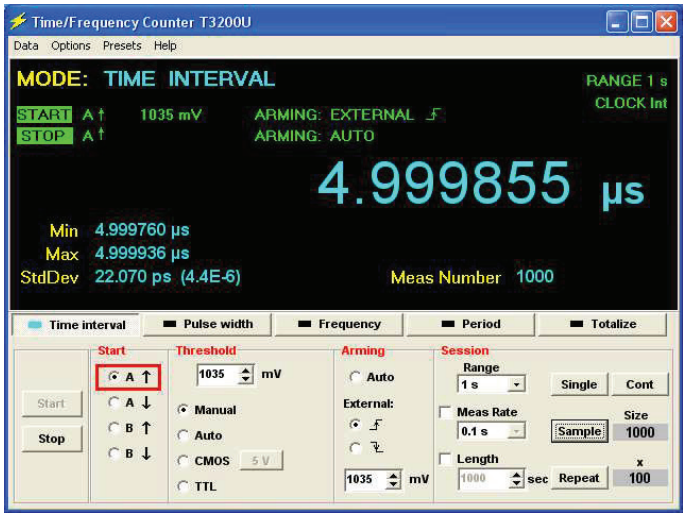

Figure 4. Example of the virtual front panel of the counter operating in the Time Interval mode

The fundamental measurement mode is the Time Interval, which allows to measure of intervals with the resolution up to 1.2 ps and precision below 10 ps. The thresholds of the input comparators can be set manually in the range –4V to 4V, or can be preset on the fixed (TTL or CMOS) level. The threshold level can also be adjusted automatically.

The Pulse Width mode allows for measurement of the width of pulses applied to the input START or STOP. The polarity of pulses (active edges) and threshold level are defined in the same way as in the Time Interval mode.

In the Frequency mode, the signal frequency up to 3.5 GHz is measured with the use of the reciprocal method by measuring the time interval consisting of a known integer number of signal periods, calculating the duration of a single period, and calculating its reciprocal.

In the Period mode the measurements are performed in a similar way as in the Frequency mode.

In the Totalize mode the input pulses are counted within a preset time gate. The duration of the gate may be selected from 1 μs to 10 s, or not set (Open Gate mode). For each gate the number of counted pulses and the respective mean frequency in pulses per second are displayed.

V. WANDER MEASUREMENT

A commonly used parameter for characterizing the wander is the Time Interval Error (TIE) [11]. The maximum value of TIE (MTIE), computed from an array of TIE data, can characterize the frequency offsets and phase transients of a tested signal to obtain a clear view of quality of relevant electronic apparatus or systems. The time interval counters offer possibility of precise measurement of TIE, MTIE and Time Deviation (TDEV) related to wander.

The time error function TE(t) of a clock (in standards also $x(t)$), with respect to a frequency standard, is the difference between the time of that clock and the reference time

$$x(t) \equiv \mathrm{TE}(t) = \mathrm{T}(t) - \mathrm{T}_{\mathrm{ref}}(t).$$

Referring to figure 5, the sampling interval τ_0 is specified as follows. It begins with the START ENABLE signal generated to allow measurement of the first TE (marked by TE_1) between the nearest zero-crossing of the tested signal (of frequency f_t) and that of the reference signal (of frequency f_r). Since the interval τ_0 is generated by the counter asynchronously with reference to the tested signal, the time lag from beginning of the sampling interval to the START moment (t_1) is randomly variable within the range $(0 - 1)T_t$. That measurement is repeated in the end of the interval τ_0 and the second TE equal to the delay TE_2 is measured.

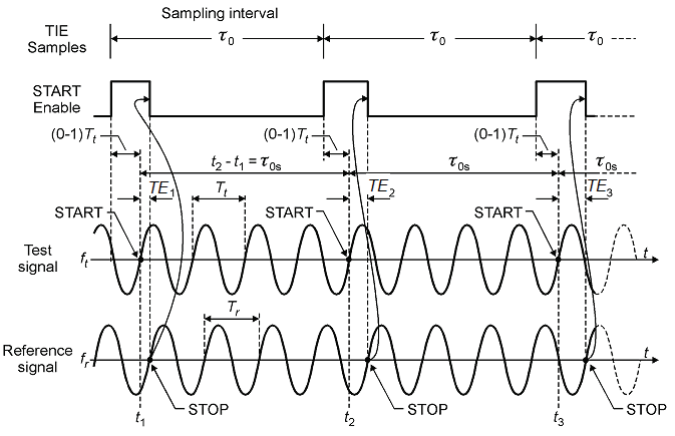

Figure 5. Measurement of Time Interval Error

The TIE sample is defined over the sampling interval τ_0 as the difference $TE_2 - TE_1$ measured in both ends of the synchronized sampling interval $\tau_{0s} = t_2 - t_1$. The worst-case difference between the interval τ_0 and τ_{0s} is $\pm T_t$.

We can observe a train of 'TE samples' (TE_1, TE_2,...) and a train of 'TIE samples' of the form

$$\mathrm{TIE}_1(\tau_0) = TE(t_2) - TE(t_1) = TE_2 - TE_1$$
$$\mathrm{TIE}_2(\tau_0) = TE(t_3) - TE(t_2) = TE_3 - TE_2$$
.....

The result of TIE measurement over the observation interval τ is the root-mean-square value $\mathrm{TIE}_{\mathrm{rms}}(\tau)$ calculated from a finite number N of TE samples collected within that interval. Utilizing the number $n = N - 1$ of the TIE(τ_0) samples

$$\mathrm{TIE}_{\mathrm{rms}}(\tau_0,\tau) = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(\mathrm{TIE}_i)^2}$$

This is shown on the display panel (fig. 6) after collecting data for a specified observation interval. The maximum time interval error (MTIE) is defined as the maximum peak-to-peak variation of TE in the all possible observation intervals $\tau = n\tau_0$ within a measurement period T. The array of N samples of TE (collected within an observation interval of $\tau = n\tau_0$) may be searched by software to find the minimum value $\mathrm{TE}_{\mathrm{min}}$ and the maximum value $\mathrm{TE}_{\mathrm{max}}$. Then $\mathrm{MTIE}(\tau_0,\tau) = \mathrm{TE}_{\mathrm{max}} - \mathrm{TE}_{\mathrm{min}}$.

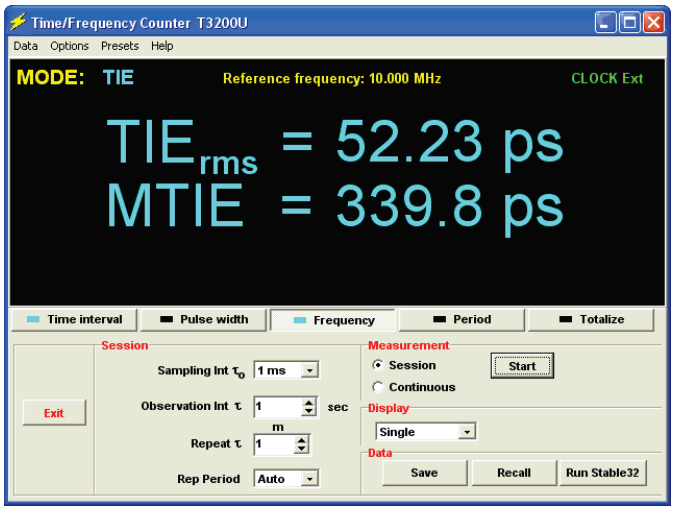

Figure 6. Virtual front panel of the counter operating in the TIE mode

In many telecommunication applications, following the ITU Recommendations there is a need to check if the measurement data conform to the requirements specified in a relevant ITU document. In such a case a relevant limit mask can also be displayed. An example is shown in fig. 7, where the mask defined in the ITU Recommendation G812 (clock 1) is displayed. It allows for easy checking the quality of the clock under test.In accordance with ITU-T Recs G.813 and G.812 the maximum sampling interval is limited to $\tau_{0\mathrm{max}} = 1/30$ s ≈ 33 ms. The counters provide the τ_0 magnitude selectable in 1-2-5-10-20-33ms sequence.

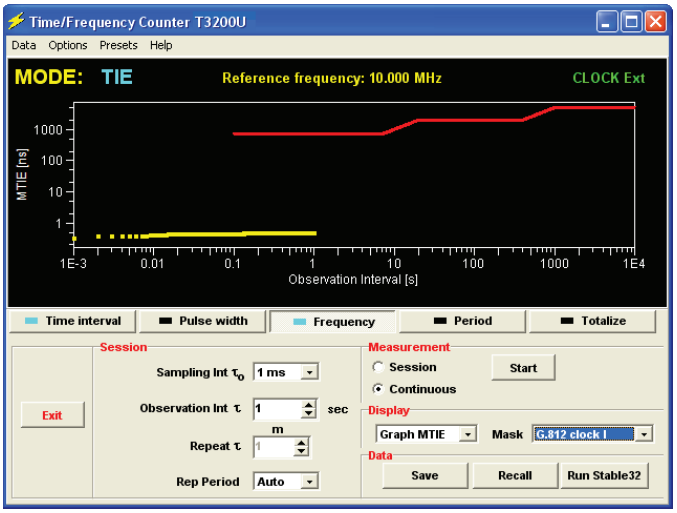

Figure 7. Graph MTIE(τ) with limit mask (G.812 clock 1)

VI. EXAMPLE TEST RESULTS

The measurement uncertainty of the successive generations of our time counter is shown in figure 8. As a reference signal of 10 MHz we used rubidium frequency standard FS725 (*Stanford Research Systems*). As sources of time intervals we used in turn three delay generators: GFT1004 (*Greenfield Technology*) for the range 10 ns – 200 ns, 81130A (*Hewlett Packard*) for the range 500 ns – 5 μs and T5300U (*Vigo System*) for the time intervals longer than 10 μs. The use of three generators allowed to select their best operation ranges (the lowest jitter) for delay generation.

The time counter with a single tapped delay line in SIS (T2700U), implemented in 90 nm CMOS technology (*Spartan-3*), provides measurement uncertainty below 50 ps. By the use of the equivalent coding line composed of two delay lines implemented in the same technology (T3200U)

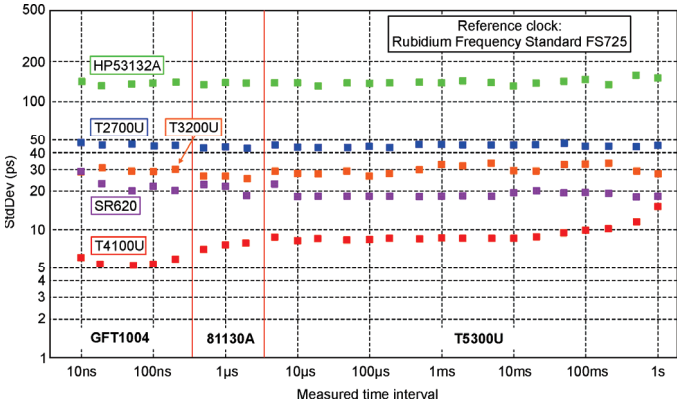

Figure 8. Comparison of the precision (standard measurement uncertainty) of succesisive versions of our time counter (T2700U with a single coding line, T3200U with a double coding line and T4100U with multiple coding lines) and selected commercial time counters (HP53132A, *Hewlett-Packard* and SR620, *Stanford Research Systems*)

the uncertainty was diminished below 35 ps. The newest counter with 16 delay lines in SIS (T4100U), implemented in 45 nm CMOS technology (*Spartan-6*), allows to achieve the precision better than 10 ps within the range of 100 ms. The latter results are much lower than derived from popular and commonly used counters such as HP53132 (*Hewlett Packard*) and SR620 (*Stanford Research Systems*).

VII. CONCLUSIONS

The described time counters allow precise measurements of long time intervals with picosecond accuracy at a lower price than standalone counters of comparable parameters. The natural applications of the counters are advanced systems for time keeping, laser ranging and navigation. They can also be used in industrial and research laboratories, and in ATE systems. Thanks to the use of programmable devices (FPGA and CPLD) the counter boards can be customized to match the user applications.

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